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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 20031215

Application Number: 09/821,554
Filing Date: March 29, 2001
Appellant(s): CHANG ET AL.

Tung & Associates
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 22, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(2) Related Appeals and Interferences

The statement of the status of the claims contained in the brief is correct.

(3) Status of Claims

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(4) Status of Amendments After Final

The summary of invention contained in the brief is correct.

(5) Summary of Invention

The appellant's statement of the issues in the brief is correct.

(6) Issues

Appellant's brief includes a statement that claims 1, 3-4. 7-8. 10-11 and 14-15 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-7 1and 8-15 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,291,334 B1	SOMEKH	9-2001
6,004,883	YU ET AL.	12-1999

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 1, 3, 4, 6, 7 and 8, 10, 11, 13, 14, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Somekh (US 6,292,334 B1).

As pertaining to claims 1, 4, 8, and 11 Somekh teaches a method of forming an aperture through a dielectric layer. The method comprises:

". . . depositing a first dielectric layer, such as a fluorinated silicate glass (FSG) layer, on a substrate," (column 2, lines 51-23 and (column 3, lines 36-38 and FIGS. **4a-4f**), which reads on,

providing a substrate;

"depositing a low k dielectric etch stop (**14**, which is the same as applicant's first dielectric layer), such as an α-FC layer, on the first dielectric layer, patterning the etch stop (**14**) to define the contacts/vias," (column 2, lines 53-57; column 3, lines 43-50) and " . . . α-FC (dielectric constant ~ 2.8) . . ." (column 4, lines 14-17), which reads on,

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

"After low k etch stop **14** has been etched to pattern the contacts/vias and the photoresist has been removed, a second dielectric layer **18** (such as FSG, see column 2, lines 56-57 and which is the same as applicant's blanket dielectric layer) is deposited over etch stop **14** . . . as shown in FIG **4d**" (column 3, lines 52-56). FIG **4d** also shows that dielectric layer **18** fills the via in layer **14** as well as covers layer **14**. Somekh teaches, "Also, dielectric material having a lower dielectric constant than that of silicon dioxide (dielectric constant ~ 4.0) are being seriously considered for use in production devices. One example of these dielectric material is fluorine-doped silicon dioxide also known as fluorine-doped silicon glass (FSG) (dielectric constant ~3.5-3.7)" (column 1, lines 33-39). Hence, the aforementioned reads on,

forming upon the patterned first dielectric layer (**14**) and filling the via a blanket second dielectric (**18**) material formed of a second dielectric material having a second dielectric constant of less than about 4.0;

"The second dielectric layer **18** is then patterned to define interconnect lines **20** (same as appellant's trench), . . . with a photoresist layer **22** as shown in FIG. **4e**" (column 3, lines 56-59 and column 2, lines 56-58), which reads on,

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than at least in part overlapping an areal dimension of the via;

FIG. **4f** shows no layer between the patterned first dielectric layer **14** and the blanket second dielectric layer **18**. FIGS. **4e** and **4f** show that the opening **16** (aperture) in dielectric layer **14** is contiguous with a patterned dielectric layer **18** interconnect (same as appellant's trench) that is filled to form interconnects (same as appellant's trench) **26** (**FIG. 4h** and column 5, lines 15-18). Somekh teaches, "The interconnects are etched down to the etch stop (**14**) in the final etch step, and then the etching continues past the patterned etch stop to define the contacts/vias" (column 2, lines 59-62). "The interconnects and contacts/vias are then etched using reactive ion etching or other anisotropic etching techniques to define the metallization structure (i.e., the interconnect and contact/via) as shown in FIG. **4f**" (column 3, lines 59-63 and column 2, lines 59-60), which reads on,

etching while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop with the anisotropic etch method, in claims 1, 4, 8, and 11; and further read on,

forming within the aperture a contiguous patterned conductor interconnect and patterned conductor stud layer, as in **claim 8**.

Somekh further teaches:

the α-FC etch stop layer and the second α-FC layer (column 4, lines 31-32 and column 4, lines 62-66), and the α-FC has a dielectric constant of ~2.8 (column 4, lines 15-16), and alternative carbon based films such as parylene (column 3, lines 43-46 and column 5, lines 33-41), which read on the patterned first dielectric layer and the blanket second dielectric layer are formed from a separate dielectric material selected from the group consisting of amorphous carbon dielectric materials, as in **claims 3 and 10**;

a second α-FC layer (same as a appellant's blanket second dielectric layer) of 5000 Å (column 4, lines 61-62 and column 3, lines 54-56), falls within the range of and reads on,

a dielectric layer having a thickness from 4000 to 7000 angstroms as in **claims 6 and 13**;

a photoresist layer is formed over the α-FC etch stop layer and the second α-FC layer (column 4, lines 46-48 and column 4, lines 63-66), reads on the patterned mask layer is selected from the group consisting of patterned photoresist mask layers, **in claims 7 and 14;** and

the patterned dual damascene structure (same as applicant's contiguous patterned conductor interconnect and patterned conductor stud layer) is filled with copper and planarized by chemical mechanical polishing (column 5, lines 17, 18, and 24-26; and FIG. **4h**), which reads on, the contiguous patterned conductor interconnect and patterned conductor stud layer is formed within the aperture while employing a chemical mechanical polish (CMP) planarizing method, as in **claim 15**.

2. Claims 2, 5 and 9, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh (US '334 B1) as applied to claims 1 and 8 respectively above, and further in view of Yu et al. (US 6,004,883).

Somekh differs in failing to specify the microelectronic fabrication selected group wherein a substrate is employed, in **claims 2 and 9**.

Yu teaches, "a substrate employed within a microelectronics fabrication including but not limited to a semiconductor integrated circuit microelectronics fabrication, . . ." (column 7, lines 38).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Somekh by using the microelectronic fabrication method as taught by Yu for the purpose forming within a microelectronics fabrications low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers, with attenuated process complexity (column 6, lines 6-11).

Somekh differs in failing to teach a first dielectric layer is formed to a thickness from 4000 to 10,000 angstroms, in **claims 5 and 12.**

Yu teaches a first dielectric layer having a thickness of from 5000 to about 9000 angstroms (column 7, lines 55-58), which falls within the range of 4000 and 10,000 angstroms.

Hence it is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Somekh by using a dielectric layer having a thickness as taught by Yu for the purpose of forming within a microelectronics fabrications low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers, with attenuated process complexity (column 6, lines 6-11).

(11) Response to Argument

Appellant argues that Somekh's low k etch stop layer **14** differs from appellant's patterned first dielectric layer; disagree that Somekh's low k etch stop layer **14**

corresponds with appellant's first dielectric layer within appellant's damascene structure, and argues that Somekh's first dielectric layer is layer **10.**

Appellant's argument is unpersuasive because Somekh's layer **14** is a low k dielectric layer having a dielectric constant ~2.8 (column 4, lines 14-17), is patterned and etched to form a via (column 3, lines 46-54), which meet the limitation of " forming a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via" as in the present claims 1, 4, and 8.

The Appellant's also argue that Somekh's blanket first dielectric layer **10** and blanket second dielectric layer **18** are formed of a fluorosilicate glass (FSG) dielectric material (col. 4, lines 20-25 and 60-65) and Somekh's blanket second dielectric layer **18** will inherently not provide an intrinsic etch stop with respect to Somekh's blanket second dielectric **18**, as required in claim 1, amended claim 4, claim 8 and amended claim 11.

Appellant's argument is unpersuasive because Somekh's dielectric **18** is formed of (FSG) having a dielectric constant ~3.5 - 3.7 (column 1. lines 33-39); fills the via formed in and covers the low k etch stop layer **14** (same as a appellant's first dielectric layer having a dielectric constant less than 4.0, column 4, lines 54-56); is patterned and etched to form a interconnect lines (trench) (column 4, lines 59-59), and would therefore be the same as appellant's blanket second dielectric layer as in the present invention. "The interconnects lines (trench) are etched down to the etch stop (**14**) in the

final etch step, and then the etching continues past the patterned etch stop to define the contacts/vias" (column 2, lines 59-62), which shows forming a trench in dielectric layer **18** by etching until the etch stop layer **14** is reached, thereafter, etching is continue to etch the via in layer **14**. Since Somekh shows no layer between the patterned first dielectric layer **14** and the blanket second dielectric layer **18** (see FIG. **4f**), and uses the same method in etching the same materials as the claimed invention, then using Somekh's etching method in etching the same layers as claimed in the present invention would result in,

an intrinsic etch stop within the anisotropic etch method, in **claims 1, 4, 8 and 11.**

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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ltue
December 15, 2003

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